



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

KIMURA et al

Atty. Ref.: 1035-471

Serial No. 10/670,194

Group: 1632

Filed: September 26, 2003

Examiner:

For: **CHIP-STACK SEMICONDUCTOR DEVICE AND
MANUFACTURING METHOD OF THE SAME**

* * * * *

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Sir:

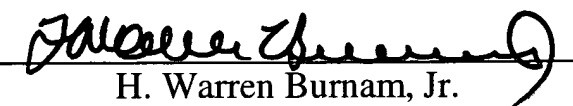
SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Further to applicants' Supplemental Information Disclosure Statement of January 9, 2004, applicants herewith submit a further corrected Form PTO-1449 (i.e., the U.S. reference which was omitted on the PTO-1449 submitted January 9, 2004 has been added and the "ABSTR" has been moved into the "translation - yes" column for the two Japanese references).

Respectfully submitted,

NIXON & VANDERHYE P.C.

February 4, 2004

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